50 GHz SAMPLER HYBRID
UTILIZING A SMALL SHOCKLINE AND AN INTERNAL SRD

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ABSTRACT

A $50\,GHz$ sampler whose performance is a result of the addition of a small GaAs nonlinear transmission line is described. The compact hybrid microcircuit also features a step recovery diode (SRD), a microstrip-to-slotline balun, and a GaAs integrated sampling bridge to form a complete sampling subsystem.

INTRODUCTION

Small and compact sampling downconverters have found many applications in phase locked synthesizers, frequency counters, network analyzers, and oscilloscopes [1-4]. The use of silicon step-recovery-diodes, thin film technology, and beam lead integrated diode circuits has provided broadband operation to $40\,GHz$ in some of these applications. The ability to push beyond $40\,GHz$ is now primarily limited by the 35-45ps falltime of the SRD used to strobe the sampling gate. To decrease the falltime of the SRD output pulse and increase the bandwidth of the sampler without significantly sacrificing conversion efficiency has led to the investigation of nonlinear transmission lines. Nonlinear transmission lines for pulse steepening have been proposed for many years [5], but no demonstrations of small, high efficiency shocklines with practical application have been published to date. If a pulse is allowed to propagate over a sufficient length of nonlinear transmission line then a shock front will form on the leading edge of the pulse. Hence, for economy of terminology we will also use the term shockline when referring to nonlinear transmission lines. Our focus in shockline design was not the fastest possible output pulse-edge slew rate, but rather high efficiency power transfer with a 3:1 to 4:1 decrease in pulse falltime in a length of line as short as possible. To investigate possible improvements in performance, the sampler structure described by Gibson [1] was modified to accommodate a short nonlinear transmission line.

NONLINEAR TRANSMISSION LINES

A nonlinear transmission line is a high impedance transmission line with varactor diodes placed in shunt at various intervals along its length. For the purposes of this discussion, a shockline is constructed from N identical cells in which each cell contains a discrete varactor centered in a length d of transmission line. The voltage variable capacitance $C_j(V)$ leads to a voltage-dependent time delay $\tau(V) = \sqrt{L\,(C + C_j(V))}$ where L and C are the inductance and capacitance, respectively, of the unloaded (i.e. no varactors) transmission line in each cell. If $C_j(V)$ decreases with increasing voltage then higher voltage portions of a pulse will propagate faster than lower voltage portions leading to steepening of the pulse's leading edge and slowing of its trailing edge. The minimum 10%-90% transition time $t_{\min}$ that the shockline can generate and propagate is limited by a complicated interaction of the following:

1. the cutoff frequency due to the periodic structure of the shockline $\omega_c = 2/\sqrt{L\,(C + C_j(V))}$,
2. the resistive cutoff frequency $\omega_{cr} = 1/R_s\,C_j(V)$ where R_s is the series resistance of the varactor diode, and
3. the series resonant frequency $\omega_{cs} = 1/\sqrt{L_s\,C_j(V)}$ due to the parasitic series inductance L_s of the connections to the varactor diode.

To achieve large amounts of pulse steepening in a short length of line, hyperabrupt varactors are used since they provide greater changes in time delay with voltage. However, as a varactor diode becomes more hyperabrupt its series resistance will increase resulting in a decrease of ω_{cr} and an increase in $t_{\min}$. In contrast to the work of Madden, et. al. [6], our goal in this instance was to produce $10ps$ transitions in as short a length of line as possible. As a result, very hyperabrupt varactors were designed and used. Hyperabrupt varactor characteristics are in general given by $C_j(V) = C_{jo}/(1 + V/V_b)^\gamma$ where V is the applied reverse-bias voltage, $V_b \approx 0.9\,V$, and $\gamma > 1$. Hyperabrupt varactor material was grown on semi-insulating GaAs wafers using molecular beam epitaxy. The resulting varactors became fully depleted at $10V$ with $1.5 < \gamma < 2$ from $1V$ to $8V$ and with breakdown voltages in excess of $15V$.

To maintain a reasonable impedance level with $C_j(V) >> C$ requires an unloaded line impedance as high as possible. For purposes of integration either coplanar waveguide (CPW) or coplanar strip (CPS) technology is used due to the ease of one-sided-only processing and the low parasitic connections which can be made to the varactors. As the spacing between the conductors is increased, the limits to which CPW or CPS impedance can be raised are set by the increasing probability of radiation losses [7] and the increasing parasitic inductance L_s of the connections to the varactors. The practical upper limit for CPW characteristic impedance on GaAs is 90Ω and for CPS on GaAs is approximately 150Ω [8].

The shocklines used in this application were based on CPS transmission lines which are compatible with the slotline structure utilized in the the local oscillator path of the sampler. This particular shockline used two series-connected varactors in each cell to avoid forward conduction of the varactors during the charge-storing cycle of the SRD and to accommodate the large $19V$ peak pulse voltage generated by the SRD. There are $N = 27$ cells in this shockline and the length d of the CPS transmission line in each cell is $50\mu m$. Beam leads are used for input and output connections and the chip size is $0.31mm \times 1.64mm$. Using a computer program to solve the two-dimensional Poisson equation, the unloaded impedance and propagation velocity of the CPS transmission line was computed to be approximately 140Ω and $1.1 \times 10^{10}\ cm/sec$, respectively, which included the effects of the package walls and of the underlying alumina substrate to which the chip is bonded. Fitting measured $C_j(V)$ characteristics of large-area varactor diodes to the ideal diode equation and then scaling to the diode area used in the shockline yielded $C_{jo} = 500fF$ and $\gamma = 1.7$. The measured series resistance of each varactor was $R_s = 20\Omega$ and the total series inductance connecting the two varactors to the CPS transmission line was estimated to be $L_s \approx 30pH$. SPICE simulations predicted output 10%-90% falltimes of $8ps$-$10ps$ when using $40ps$ 10%-90% falltime input pulses. Large-signal characterization was initially performed using individually packaged shocklines fabricated with CPW transmission lines so that shockline performance could be measured without the masking influences of the sampler's balun structure. The large-signal performance of the CPS shocklines were not measured individually but as part of complete samplers.

SAMPLER DESCRIPTION

The sampling subsystem consists of a $2.5in. \times 3in.$ printed circuit board which contains the local oscillator (LO) amplifier, the intermediate frequency (IF) amplifier, the sampler hybrid, and all necessary bias circuitry. A block diagram is shown in Figure 1. The impedances of the RF and LO inputs and the IF output are all 50Ω, and the gains of the LO and IF amplifiers are 11 dB and 32 dB, respectively.

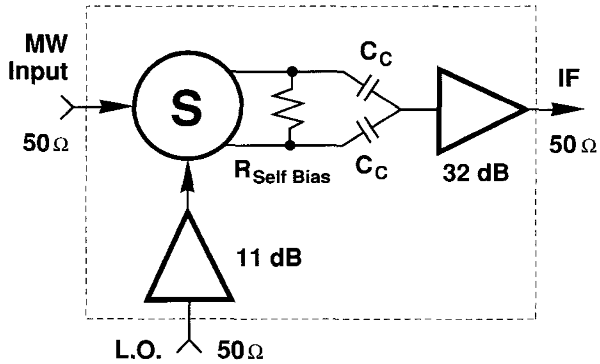

Figure 1. Block diagram of the sampling subsystem.

The sampler hybrid circuit is contained within a $0.75in.$ diameter gold-plated aluminum package and consists of the SRD and its input matching network, a microstrip-to-slotline balun, and a beam lead GaAs integrated diode circuit on a supporting alumina substrate. As shown schematically in Figure 2, the sampling diode chip contains sampling diodes D1 and D2, 100Ω RF terminating resistors R_T, $2pF$ silicon nitride hold capacitors C_H, and 50Ω IF output resistors R_H. The RF signal is introduced via a $2.4mm$ connector through the floor of the hybrid's package and is ribbon-bonded to the CPW transmission line on the alumina substrate. Also entering through the floor of the package are the IF output pins and the LO drive signal for the SRD. An SRD pulse is launched into a microstrip line which overlays the main alumina substrate. A slotline is formed in the ground plane of the microstrip to produce a balun which launches a balanced pulse towards the sampling diodes.

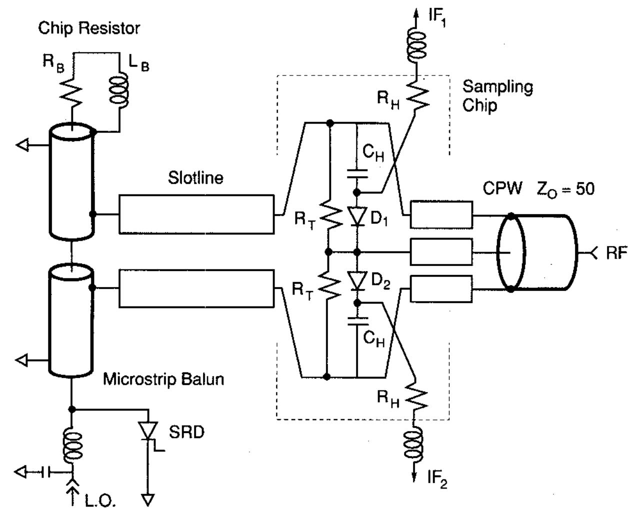

Figure 2. Schematic of the original sampler.

The nominal amount of time that the sampling diodes are turned on is set by the round trip time between the plane of the sampling diodes and the slotline short formed by the CPW RF input port [9]. This time interval, the gate time, is adjustable by changing the reverse DC bias applied to the sampling diodes via the self-bias resistor connected between the two IF output pins. Reducing the gate time to increase the bandwidth of the sampler can be accomplished by increasing the self-bias resistor and/or by shortening the length of the CPW input transmission line. However, this is at the cost of reducing the sampling-diode gate current which increases the sampling-diode impedance and degrades the sampler conversion efficiency. Using a shockline to significantly increase the leading-edge speed of the pulse driving the sampling diodes allows short gate times but with much higher sampling-diode gate current and as a result can improve conversion efficiency as well as bandwidth.

In order to accommodate the addition of the shockline, the alumina substrate was stretched in the area between the balun and the sampling-diode integrated circuit as shown in Figure 3. With respect to the sampler described in [1] the following additional changes were made: First, the outer edges of the slotline were tapered inward to connect to the CPS structure of the shockline. Second, the balun termination was modified by replacing the 50Ω chip resistor R_B with a short circuit ribbon bond to the microstrip ground plane which increased the current transferred from the microstrip to the slotline. Third, the slotline open circuit was modified by adding termination resistors which increased the LO to RF isolation. Finally, the input coplanar waveguide had to be shortened by 30% to remove an unwanted resonance that was occuring at 50 *GHz*. This last change had the additional effect of reducing the round-trip time between the sampling diodes and the slotline short. Figures 2 and 4 show schematically the differences between the original and shockline-enhanced samplers.

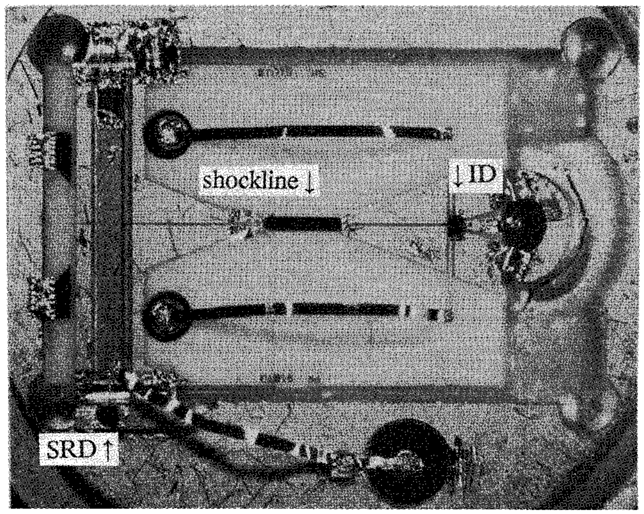

Figure 3. Photograph of the sampler hybrid. The thin film circuit is 6.5 $mm \times 10 mm$. At the left, the SRD is mounted just below the microstrip-to-slotline balun. The two IF output pins protrude through the thin-film circuit. The LO input is at the bottom and the RF input is at the right side of the photograph. ID = Integrated Diode sampling chip.

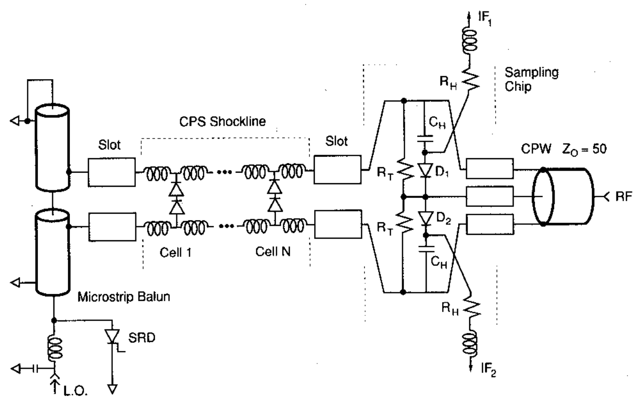

Figure 4. Schematic of the shockline-enhanced sampler.

MEASURED RESULTS

Frequency responses of the original and shockline-enhanced samplers were measured from $2GHz$ to $60GHz$ using LO frequencies of $300MHz$, $325MHz$, and $350MHz$. The LO power input at the printed-circuit-board connector was $+14dBm$ resulting in a $+25dBm$ signal to the SRD. The $-10dBm$ RF input power was supplied by an HP8340 synthesized sweeper and two millimeter-wave source modules, the $26.5GHz$ - $40GHz$ HP83554A and the $40GHz$ - $60GHz$ HP83556A. Using a self-bias resistance of $287k\Omega$ for the original sampler, the conversion loss at $2GHz$ was $-8dB$ when measured from the RF port to the IF output port of the printed circuit board (Figure 1). Using a $51k\Omega$ self-bias resistor for the shockline-enhanced sampler yielded a $3dB$ improvement in conversion loss from $2GHz$ to $40GHz$ with increasing improvement beyond $40GHz$ as shown in Figure 5. Reduction of the self-bias resistance value by more than a factor of five is also indicative of an improvement in dynamic range.

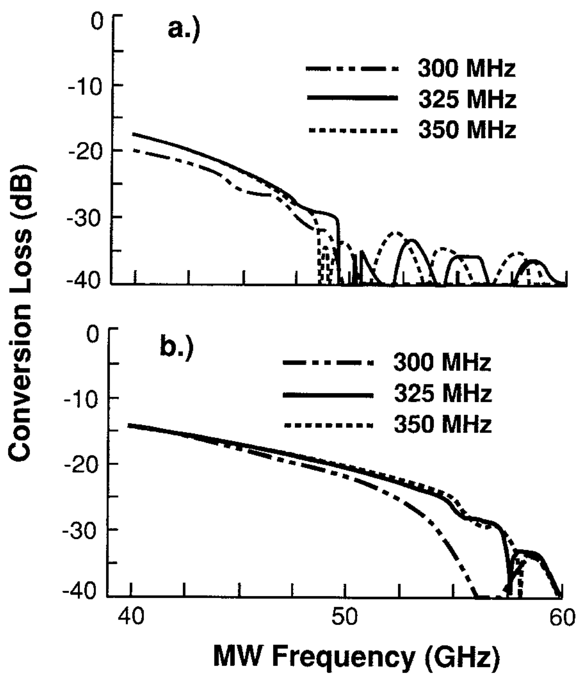

Figure 5. Measured frequency response of (a) the original sampler and (b) the shockline-enhanced sampler.

CONCLUSION

We have shown the viability of using very short, low loss nonlinear transmission lines to improve the conversion efficiency and bandwidth of a small, compact hybrid sampler. The shockline-enhanced sampler had a usable bandwidth of $55GHz$, $10GHz$ greater than the sampler without a shockline. In addition, the conversion efficiency of the shockline-enhanced sampler was improved over the full measured frequency range of 2 - $60GHz$ when compared to the response of the sampler that did not use a shockline.

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